

501.41197CX1

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant(s): T. TAIRA  
Serial No.: (not yet assigned)  
Filed: September 26, 2003  
For: FABRICATION METHOD OF SEMICONDUCTOR  
INTEGRATED CIRCUIT DEVICE AND TESTING METHOD

**REAFFIRMATION OF CLAIM FOR PRIORITY**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

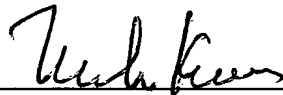
September 26, 2003

Sir:

Under the provisions of 35 USC §119 and 37 CFR §1.55, Applicants hereby claim the right of priority based on Japanese Patent Application No. 2001-075671, filed in Japan on March 16, 2001.

The certified copy of the above-referred to Japanese Patent Application was filed on March 14, 2002 in prior application Serial No. 10/096,801, filed March 14, 2002.

Respectfully submitted,



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